REMARKS

The Official Action mailed August 13, 2002 has been received and its contents carefully noted. Filed concurrently herewith is a *Request for Continued Examination (RCE)* and a *Request for One Month Extension of Time*, which extends the shortened statutory period for response to December 13, 2002. Accordingly, Applicant respectfully submits that this response is being timely filed.

Applicants note with appreciation the consideration of the Information Disclosure Statements filed on July 1, 1998; August 10, 1998; December 30, 1998; November 10, 1999; May 15, 2000; August 23, 2000; October 18, 2000; January 29, 2001; February 22, 2001; September 21, 2001; and May 20, 2002. A further IDS is submitted herewith and careful review and consideration of this IDS is requested.

Claims 16-20, 24-25, 56-61 and 74-91 were pending in the present application. Claims 76-77, 79, 84-85 and 90-91 have been canceled and claims 16, 56, and 74-75 have been amended herewith. Accordingly, claims 16-20, 24-25, 56-61, 74-75, 78, 80-83, and 86-89 are now pending in the present application, of which claims 16, 21, 56, and 74-75 are independent. For the reasons set forth in detail below, all claims are believed to be in condition for allowance.

The Official Action rejects claims 16-20, 24-25, 80 and 86 as obvious based on the combination of U.S. Patent 5,310,410 to Begin et al., U.S. Patent 5,194,398 to Miyachi et al., U.S. Patent 4,503,807 to Nakayama et al., U.S. Patent 5,200,017 to Kawasaki et al., U.S. Patent 5,292,675 to Codama, U.S. Patent 4,475,027 to Pressley, and the article "Large-Area Process for Fabrication of Poly-Si Thin Film Transistors Using Bucket Ion Source and XeCl Excimer Laser Annealing," by Kawachi et al. The Official Action further rejects claims 56-61, 81 and 87 as obvious based on the combination of Begin, Miyachi, Nakayama, Kawasaki, Codama, JP 03-286518 to Hashizume and Kawachi. Finally, the Official Action rejects claims 74-79, 82-85 and 87-91 as obvious based on the combination of Begin, Miyachi, Nakayama, Kawasaki, Codama and Kawachi.

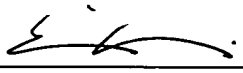
As stated in MPEP § 2143-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there

must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." *In re Kotzab,* 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

It is respectfully submitted that the present invention as recited in the claims as amended herewith is distinguished over each of the references to Begin, Miyachi, Codama, Pressley, Kawachi, and Hashizume in that none of these references disclose or suggest that an exposed surface of a semiconductor layer is irradiated with a laser light. Since the prior art of record, taken alone or in combination, fails to teach or suggest all the claim limitations, it is respectfully submitted that a *prima facie* case of obviousness cannot be maintained. Favorable reconsideration is requested in view thereof.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned attorney at the telephone number listed below.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please cancel claims 76-77, 79, 84-85 and 90-91 and amend claims 16, 56, and 74-75 as follows:

16. (Amended) An apparatus for processing a semiconductor comprising:

a first vacuum chamber;

an ion introducing apparatus [connected to said vacuum chamber] for doping a semiconductor layer formed over a substrate with a dopant impurity through an insulating film comprising oxide provided over said semiconductor layer;

an etching apparatus for etching said insulating film comprising oxide to expose a surface of said semiconductor layer, said etching apparatus connected to said ion introducing apparatus through said first vacuum chamber;

a second vacuum chamber;

a laser processing apparatus comprising a laser processing chamber and a laser for [treating] irradiating the exposed surface of said semiconductor layer with a laser light in said laser processing chamber after said [doping] etching, said laser processing chamber connected to said [ion introducing] etching apparatus through said second vacuum chamber; and

a mechanism [provided to said vacuum chamber] for transporting said substrate from said ion introducing apparatus to said laser processing chamber without exposing said substrate to the air,

said dopant impurity being made a plasma around a grid electrode of said ion introducing apparatus and being accelerated toward said semiconductor layer by a voltage applied to an anode electrode of said ion introducing apparatus.

56. (Amended) An apparatus for processing a semiconductor comprising:

a first vacuum chamber;

an ion introducing apparatus [connected to said vacuum chamber] for doping a semiconductor layer formed over a substrate with a dopant impurity through an insulating film comprising oxide provided over said semiconductor layer;

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an etching apparatus for etching said insulating film comprising oxide to expose a surface of said semiconductor layer, said etching apparatus connected to said ion introducing apparatus through said first vacuum chamber;

a second vacuum chamber;

a laser processing apparatus comprising a laser processing chamber and a laser for [treating] irradiating the exposed surface of said semiconductor layer with a rectangular shaped laser light in said laser processing chamber after said [doping] etching, said laser processing chamber connected to said [ion introducing] etching apparatus through said second vacuum chamber; and

a mechanism [provided to said vacuum chamber] for transporting said substrate from said ion introducing apparatus to said laser processing chamber without exposing said substrate to the air,

said rectangular-shaped laser light has a length greater than a width of said substrate,

said dopant impurity being made a plasma around a grid electrode of said ion introducing apparatus and being accelerated toward said semiconductor layer by a voltage applied to an anode electrode of said ion introducing apparatus.

74. (Amended) An apparatus for forming a semiconductor device comprising:

a first vacuum chamber;

an ion introducing apparatus [connected to said vacuum chamber] for doping a semiconductor layer formed over a substrate with a dopant impurity through an insulating film comprising oxide provided over said semiconductor layer;

an etching apparatus for etching said insulating film comprising oxide to expose a surface of said semiconductor layer, said etching apparatus connected to said ion introducing apparatus through said first vacuum chamber;

a second vacuum chamber;

a laser processing apparatus comprising a laser processing chamber and a laser for [treating] irradiating the exposed surface of said semiconductor layer with a laser light in said laser processing chamber after said [doping] etching, said laser processing chamber connected to said [ion introducing] etching apparatus through said second vacuum chamber; and

a mechanism [provided to said vacuum chamber] for transporting said substrate from said ion introducing apparatus to said laser processing chamber without exposing said substrate to the air,

said dopant impurity being made a plasma around a grid electrode of said ion introducing apparatus and being accelerated toward said semiconductor layer by a voltage applied to an anode electrode of said ion introducing apparatus.

75. (Amended) An apparatus for processing a semiconductor comprising:

a first vacuum chamber;

an ion introducing apparatus [connected to said vacuum chamber] for doping a semiconductor layer formed over a substrate with a dopant impurity through an insulating film comprising oxide provided over said semiconductor layer;

an etching apparatus for etching said insulating film comprising oxide to expose a surface of said semiconductor layer, said etching apparatus connected to said ion introducing apparatus through said first vacuum chamber;

a second vacuum chamber;

a light processing apparatus comprising a light processing chamber and a light source chamber for [treating] irradiating the exposed surface of said semiconductor layer with an infrared light in said light processing chamber after said [doping] etching, said light processing chamber connected to said [ion introducing] etching apparatus through said second vacuum chamber; and

a mechanism [provided to said vacuum chamber] for transporting said substrate from said ion introducing apparatus to said light processing chamber without exposing said substrate to the air,

said dopant impurity being made a plasma around a grid electrode of said ion introducing apparatus and being accelerated toward said semiconductor layer by a voltage applied to an anode electrode of said ion introducing apparatus.